

Figure 1

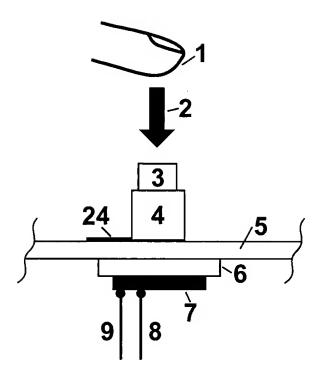


Figure 1

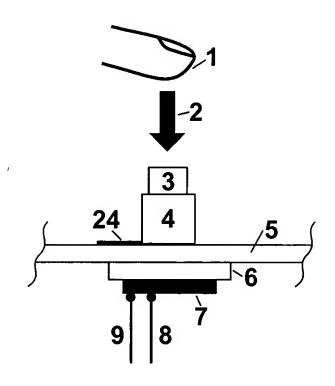


Figure 1

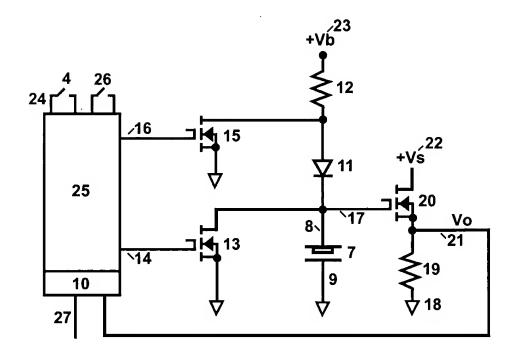


Figure 2

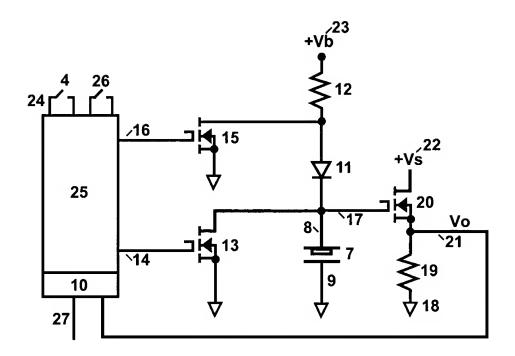


Figure 2

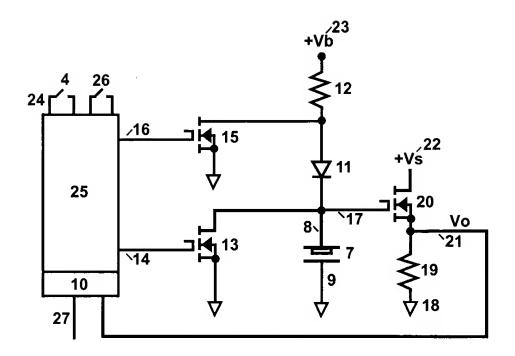
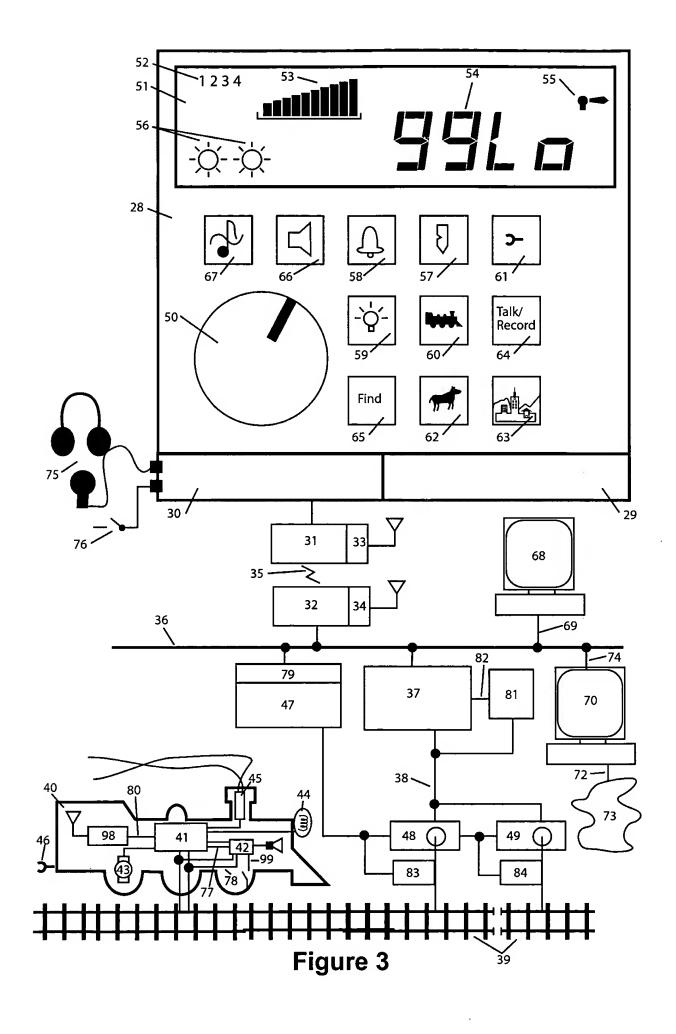
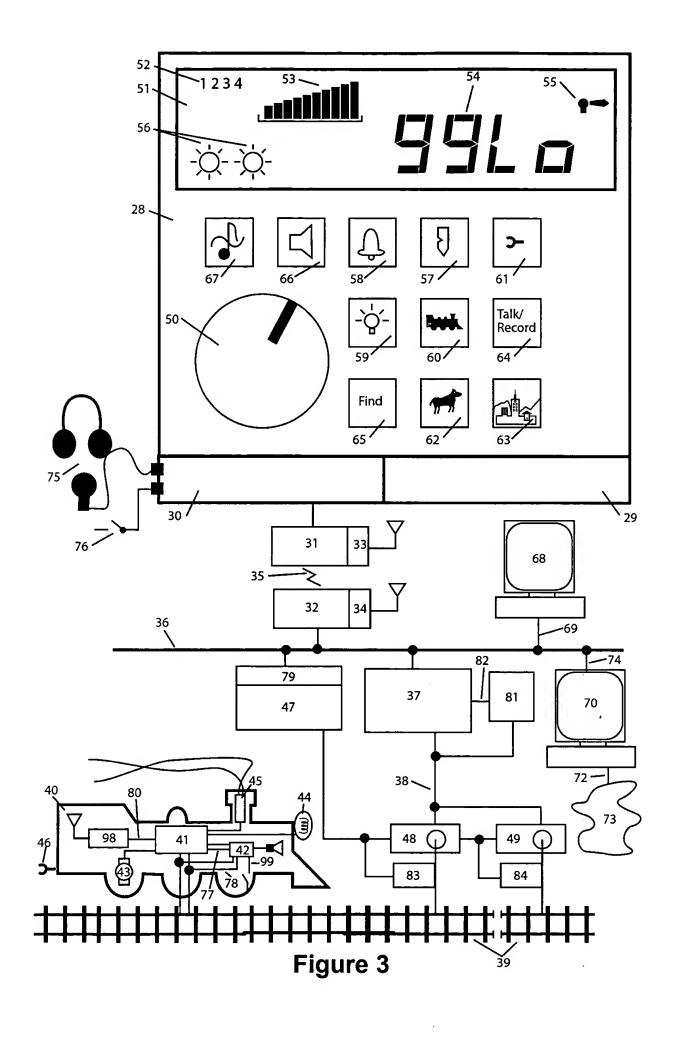
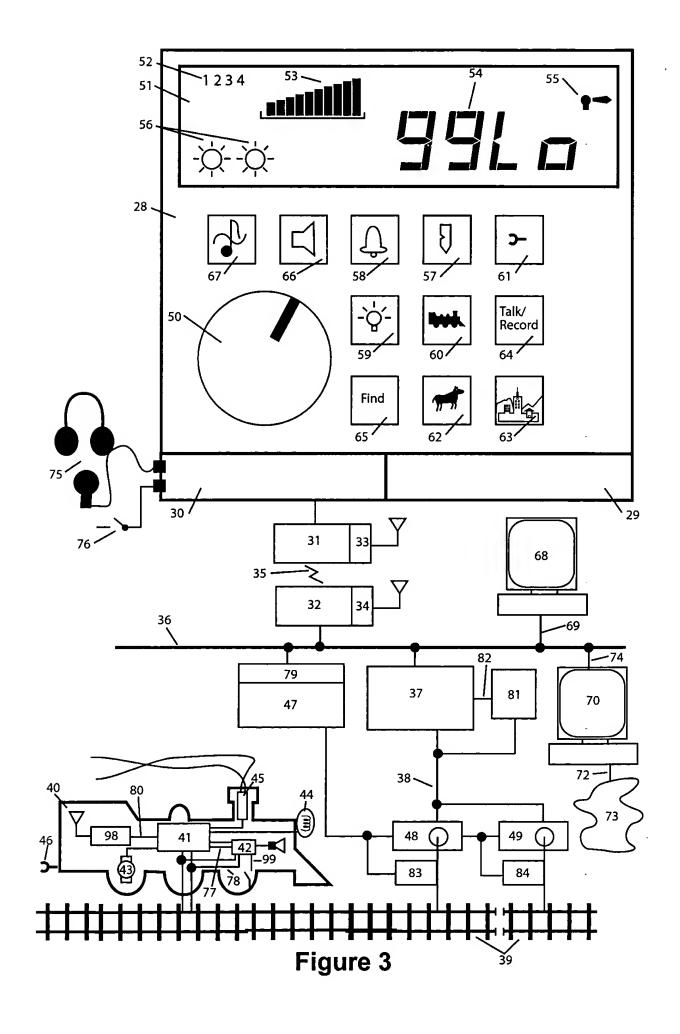


Figure 2







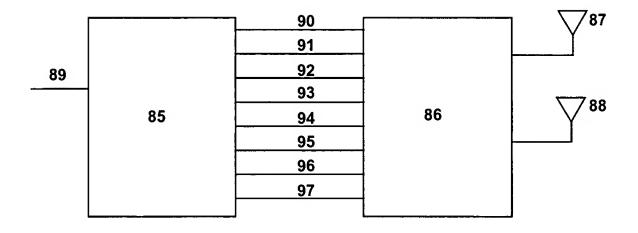


Figure 4

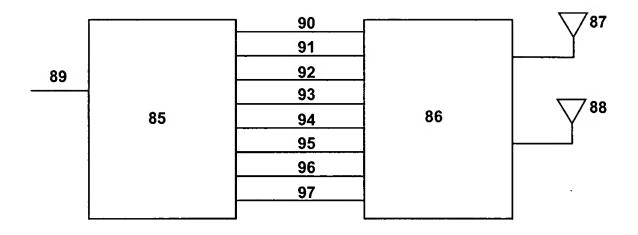


Figure 4

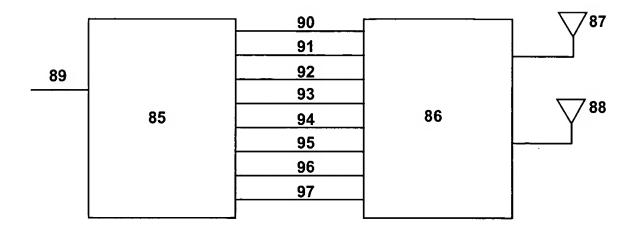
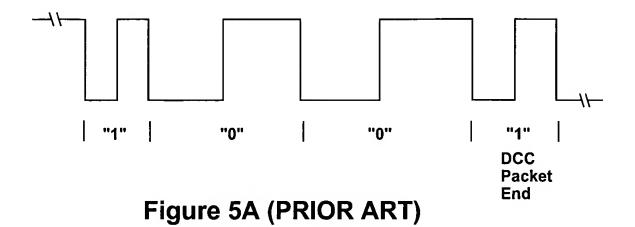


Figure 4



DCC A B Packet End

Figure 5 B

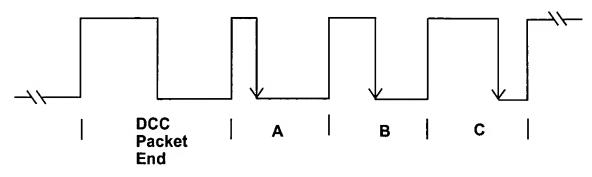


Figure 5 C

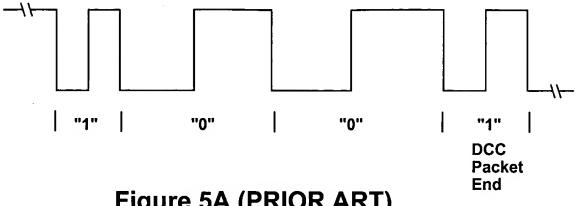


Figure 5A (PRIOR ART)

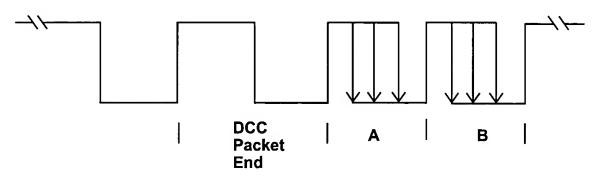


Figure 5 B

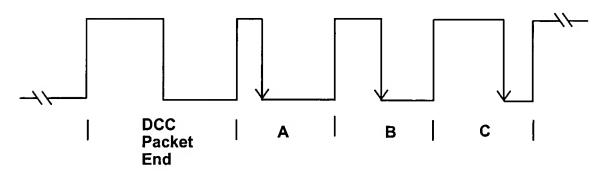


Figure 5 C

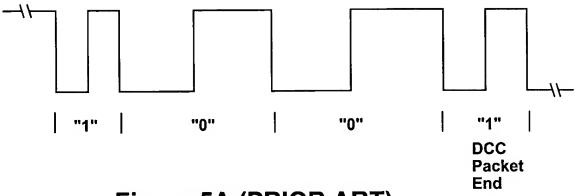


Figure 5A (PRIOR ART)

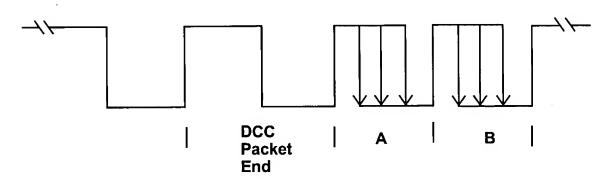


Figure 5 B

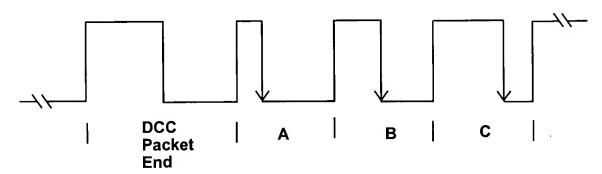


Figure 5 C